



香港公開大學 科技學院
THE OPEN UNIVERSITY OF HONG KONG
SCHOOL OF SCIENCE AND TECHNOLOGY

ELEC S411F 2020/21

Electronic and Computer Engineering Project
Final Report



Implementation of a New
Executable and Linkable Format for RISC-V

Project Number: A01

Student Name: Law Tsz Wang Leslie (12419115)

Supervisor: Dr. Angus Wong

Submission Date: 13 June 2021

Declaration of Originality

I, Law Tsz Wang Leslie, declare that this report and the work reported herein was composed by and originated entirely from me. This report has not been submitted in any form for another degree or diploma at any university or other institute of tertiary education. Information derived from the published and unpublished work of others has been acknowledged in the text and a list of references is given in the reference section.

13 June 2021

Abstract

Since RISC-V is becoming a revolutionary instruction set architecture (ISA), many technology companies have developed a strong interest in this ISA, and then invest resources for development. RISC-V will change the ecology of the entire computer architecture industry.

This project is to design a lightweight and dynamic executable and linkable format (ELF) file in order to have a more efficient file linking and execution. Then, implement the modified ELF file to RISC-V environment, to better support the future RISC-V CPU and OS development.

The GCC file is chosen to be optimized for testing that modify an ELF file can get improvement when building a RISC-V operating environment. The result showed that the optimized GNU C Compiler (GCC) file can compile almost 10% faster than the original one. It also means that the ELF file act as a main character between operating system and ISA.

Table of Content

<i>1</i>	<i>Introduction.....</i>	<i>6</i>
1.1	Project Objectives	6
1.2	Organization of the Report.....	6
<i>2</i>	<i>Literature Review.....</i>	<i>7</i>
2.1	Compete the x86 and ARM	7
2.2	RISC-V Emulator Development.....	7
2.3	Low Performance Emulator.....	8
2.4	GCC Compiler	8
<i>3</i>	<i>Methodology</i>	<i>9</i>
3.1	Read and Write ELF file	9
3.2	GNU Compiler Toolchain.....	9
3.3	64-bit RISC-V Linux on QEMU.....	10
<i>4</i>	<i>Implementation</i>	<i>11</i>
4.1	Read ELF on Terminal.....	11
4.2	Read and Write ELF Program.....	12
4.3	Section Header in ELF Files	14
4.4	Building RISC-V Environment.....	15
4.5	Compile GCC.....	16
<i>5</i>	<i>Results and Discussion</i>	<i>17</i>
5.1	GCC Compiling Result.....	17
<i>6</i>	<i>Conclusion</i>	<i>18</i>
<i>7</i>	<i>References</i>	<i>19</i>
<i>8</i>	<i>Appendix</i>	<i>20</i>

List of Figures

Figure 4.1	Result on “readelf” of GCC	11
Figure 4.2	Java program and result – Read ELF	12
Figure 4.3	Java program and result – Write ELF	13
Figure 4.4	Cover page of “64-bit ELF Object File Specification”	13
Figure 4.5	First 5 section headers of GCC	14
Figure 4.6	Help instruction and update process of Homebrew	15
Figure 4.7	Content of the GNU Compiler Toolchain	15
Figure 4.8	Screenshot when compiling GCC	16

List of Tables

Table 4.1	ELF-64 Data Types	13
Table 4.2	ELF-64 Header Structure	14
Table 5.1	Compile Time Result	17

1 Introduction

As the technology nowadays becomes more complex and more connected, the interoperability between inventors and consumers has become more important. Global standards can make the interoperability easier and more convenient, thereby driving innovation at the basic platform level.

RISC-V is a free and open instruction set architecture (ISA) which still under development. RISC-V means the fifth edition of reduced instruction set computer (RISC) architecture. It is driven through open standard collaboration of global developers, and aims to achieve freedom of design in all domains and industries, and consolidate the strategic foundation of semiconductors.

Executable and Linkable Format (ELF) is an standard, flexible and cross-platform object files participate in program linking and execution which is a binary file format commonly found in in Unix-like systems. Since the bit “zero-one” in computer system are like the DNA molecules of the organism, ELF should be the general structure of the cell. ELF supports different endianness and address-sizes, and not requires specific CPU or ISA. Therefore, implementing an optimized ELF may improve the development for RISC-V.

1.1 Project Objectives

This project is aims to modify ELF files so as to have a more efficient file linking and execution in RISC-V environment, and hopefully can participate in a very small little part of the RISC-V development.

1.2 Organization of the Report

The report is begin with section 2, the background observation of RISC-V and ELF. Some literature will be reviewed for reference on the further work on RISC-V environment. After understanding the development of RISC-V, section 3 is the methodology is listing in detail to clearly describe what will be done. Section 4 is the working process and some screenshot of the work. The testing and work result of section 4 and the further discussion is showed in section 5. The section 6 is the conclusion of the project.

2 Literature Review

RISC-V is an ISA which not optimised for any particular target, so it is suitable for all computing purposes. It is also a simple load-store architecture which can be divided into two parts, base ISA and optional extensions which means RISC-V is restricted to contain minimal instructions set but also support extensive customisation.

2.1 Compete the x86 and ARM

Comparing to X86 and ARM, the world's most famous ISA for PC and mobile. RISC-V are free and no need to pay for the IP license fee [3]. It is simpler and smaller than other ISAs, and support modularisation with multiple standard extensions. The high stability due to fixed base ISA and first extension let the developers only need to update or change the extensions. And, due to high extensibility, specific functions can be added by extensions. So, RISC-V may have a good future to compete the x86 and ARM.

In the 1980s, chip size and processor design complexity were the main limiting factors, while desktop computers and servers completely dominated the computing industry [1]. Today, energy efficiency are the main design constraints, and the computing industry is very different: the growth of smartphones or tablets running ARM exceeds that of desktops or laptops running x86. In addition, the traditional low-power ARM is entering the high-performance computer market, while the traditional high-performance x86 is entering the low-power mobile device market. Therefore, the ISA performance and energy efficiency is becoming more and more important.

2.2 RISC-V Emulator Development

RISC-V is an open and free ISA, originally developed by the University of California, and now maintained by the RISC-V Foundation, with a few companies supporting its development [4]. It is a small RISC-based architecture that divided into multiple modules supporting floating-point calculations, vector operations and atomic operations. Each module focuses on different future computing goals, such as IoT embedded devices and cloud servers.

The rapid growth and adoption of RISC-V is attracting worldwide attention. So far, Linux kernel, GCC, Clang all support it. However, the performance of all current RISC-V simulators

is very poor. Having a high-performance RISC-V emulator suitable for common architectures, x86 and ARM, in order to simplify software deployment, not only promotes its adoption and testing, but also showcases it as a useful virtual architecture. A way to implement a high-performance simulator is to use dynamic binary conversion (DBT), a technique for dynamically selecting and converting code regions during simulation [4].

This technology has been used to implement fast virtual machines (VM), simulators, debuggers, and high-level language VMs [4]. The DBT engine usually interprets the code first, and then after translating all the hot areas, most of the time is spent executing the translation area.

2.3 Low Performance Emulator

In ISA design, RISC-V has not reached a mature and stable state until now. Physically, there are several open source RISC-V CPU designs available. Although open source design can enable mass production, this type of design is still under research and experimentation, so there are currently few platforms that implement RISC-V architecture [4]. It usually takes some time to realize that the hardware of the new ISA is widely available. Until then, simulation plays a vital role, it can use the new ISA without a physical CPU available.

The main job of the ISA emulator is to convert client instructions into host instructions. The goal is to make the host execute the client's instructions. Although there are already some RISC-V simulators available, such as Spike and QEMU, they cannot achieve close to native performance, which limits their performance, so they are usually used in situations where performance requirements are not high.

2.4 GCC Compiler

GNU Compiler Collection (GCC) is the traditional compiler for most embedded systems because it supports many different ISAs on the back end. It supports many embedded processors and microcontrollers, and its status as the official GNU/Linux compiler is due to the open source model and support from the GNU/Linux community. Also for RISC-V, it is the first default compiler available [5].

3 Methodology

This project is using Java in programming for creating and modify the ELF file. In system programming, a Java SE Development Kit 16 is used for implementation of the Java platform function, integrated development environment for Java and other related function in Shell script. When emulating RISC-V environment, the GNU Compiler Toolchain recommended by the RISC-V Foundation is the main character.

3.1 Read and Write ELF file

ELF file can be found in any OS. Command line on Windows or Terminal on macOS provide an easiest way to read the ELF file information of different system or compiler file. The command line program will show the ELF header, section header and program header of the ELF file. Those information will tell the system how the ELF file creating a process image.

In order to show the above information in the binary form, a simple Java program is needed. The program can read the byte inside the ELF file, then print out in hexadecimal form which is easier to read and analysis. This program involves the conversion between the byte of the file and the binary code, as well as the conversion between binary and hexadecimal string.

As we can read the ELF in customise form, a separate program can also write a whole new ELF file by converting the information string to hexadecimal code, then convert it to binary code and write into a newly created file.

3.2 GNU Compiler Toolchain

The RISC-V foundation recommended the RISC-V GNU Compiler Toolchain which is available on Github. This toolchain is the RISC-V C and C++ cross-compiler. It supports two build modes: a generic ELF/Newlib toolchain and a more sophisticated Linux-ELF/glibc toolchain.

The original GNU C Compiler (GCC) is developed from the GNU project to create a complete Unix-like operating system as free software, to promote freedom and cooperation among computer users and programmers.

GCC has grown over times to support many different programming languages such as C (gcc), C++ (g++), Java (gcj) which is now referred to as "GNU Compiler Collection". The GNU Compiler Toolchain is for developing applications and writing operating systems which include GCC, GNU Make, GNU Binutils, GNU Debugger (GDB), GNU Autotools and GNU Bison [2].

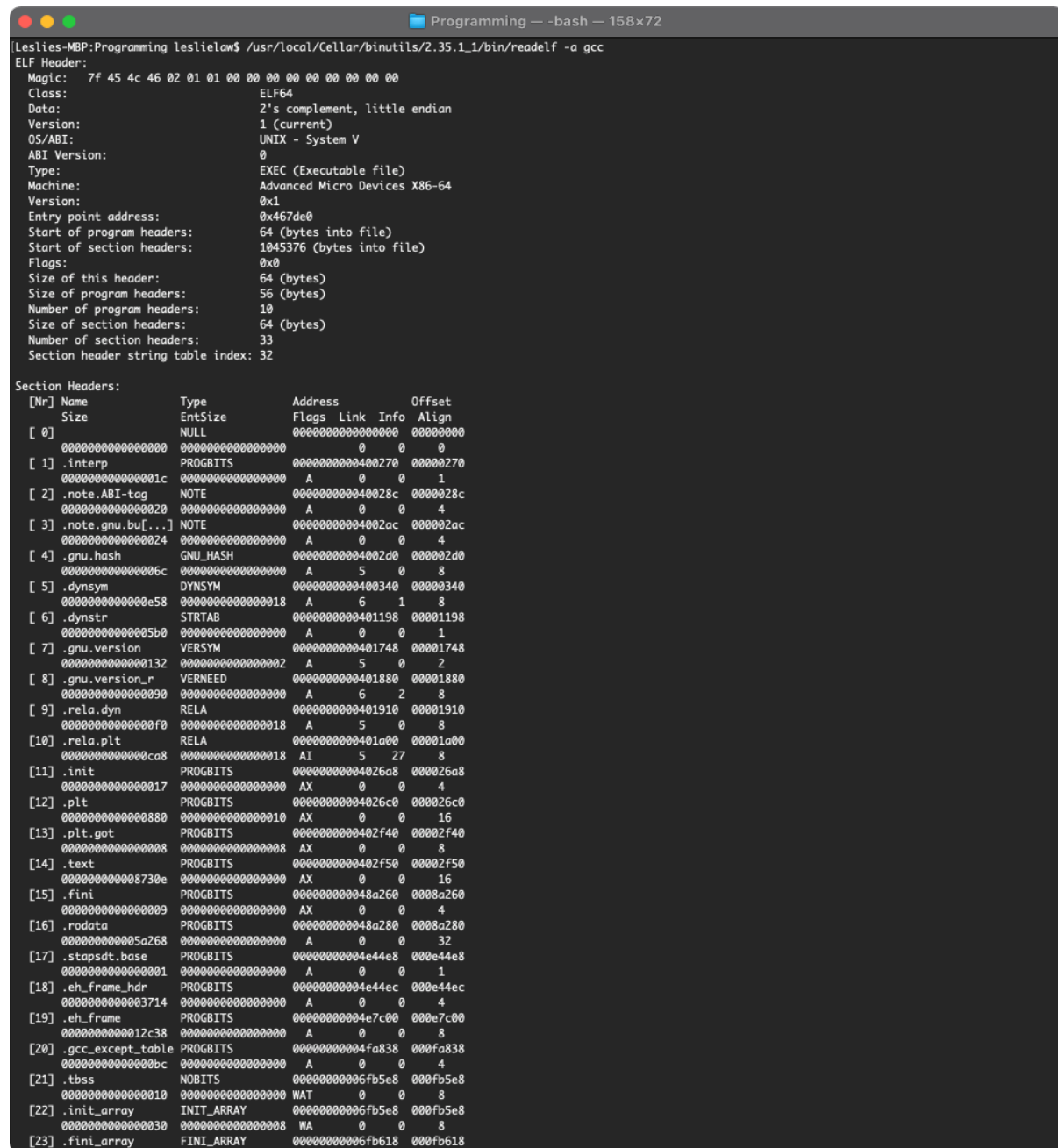
3.3 64-bit RISC-V Linux on QEMU

As the project is worked on macOS environment, a QEMU, a generic and open-source machine emulator, is needed to emulate the RISC-V environment. Booting a Linux on RISC-V QEMU can create an environment to test the customized ELF file since ELF is widely used in Linux and other Linux-like system, and Linux is suitable to run on RISC-V ISA.

4 Implementation

The implementation is doing on a Macbook Pro with macOS 11.4. The test file used is the GCC file from GNU Compiler Toolchain.

4.1 Read ELF on Terminal



```

Leslies-MBP:Programming leslielaw$ /usr/local/Cellar/binutils/2.35.1_1/bin/readelf -a gcc
ELF Header:
  Magic:   7f 45 4c 46 02 01 01 00 00 00 00 00 00 00 00 00
  Class:              ELF64
  Data:                2's complement, little endian
  Version:              1 (current)
  OS/ABI:              UNIX - System V
  ABI Version:         0
  Type:                EXEC (Executable file)
  Machine:             Advanced Micro Devices X86-64
  Version:             0x1
  Entry point address: 0x467de0
  Start of program headers: 64 (bytes into file)
  Start of section headers: 1045376 (bytes into file)
  Flags:              0x0
  Size of this header: 64 (bytes)
  Size of program headers: 56 (bytes)
  Number of program headers: 10
  Size of section headers: 64 (bytes)
  Number of section headers: 33
  Section header string table index: 32

Section Headers:
[Nr] Name           Type            Address         Offset
     Size           EntSize        Flags   Link  Info  Align
  [ 0] 0000000000000000 NULL            0000000000000000 0 0 0
  [ 1] .interp          PROGBITS       0000000000400270 00000270
     000000000000001c 0000000000000000 A 0 0 1
  [ 2] .note.ABI-tag    NOTE           000000000040028c 0000028c
     0000000000000020 0000000000000000 A 0 0 4
  [ 3] .note.gnu.bu[...] NOTE           00000000004002ac 000002ac
     0000000000000024 0000000000000000 A 0 0 4
  [ 4] .gnu.hash        GNU_HASH       00000000004002d0 000002d0
     000000000000006c 0000000000000000 A 5 0 8
  [ 5] .dynsym          DYNSYM         0000000000400340 00000340
     0000000000000058 0000000000000018 A 6 1 8
  [ 6] .dynstr          STRTAB         0000000000401198 00001198
     000000000000005b0 0000000000000000 A 0 0 1
  [ 7] .gnu.version     VERSYM         0000000000401748 00001748
     00000000000000132 0000000000000002 A 5 0 2
  [ 8] .gnu.version_r   VERNEED        0000000000401880 00001880
     0000000000000090 0000000000000000 A 6 2 8
  [ 9] .rela.dyn        RELA           0000000000401910 00001910
     00000000000000f0 0000000000000018 A 5 0 8
  [10] .rela.plt        RELA           0000000000401a00 00001a00
     00000000000000ca8 0000000000000018 AI 5 27 8
  [11] .init            PROGBITS       00000000004026a8 000026a8
     0000000000000017 0000000000000000 AX 0 0 4
  [12] .plt             PROGBITS       00000000004026c0 000026c0
     00000000000000880 0000000000000010 AX 0 0 16
  [13] .plt.got         PROGBITS       0000000000402f40 00002f40
     0000000000000008 0000000000000008 AX 0 0 8
  [14] .text            PROGBITS       0000000000402f50 00002f50
     0000000000008730e 0000000000000000 AX 0 0 16
  [15] .fini            PROGBITS       000000000040260 0000a260
     0000000000000009 0000000000000000 AX 0 0 4
  [16] .rodata          PROGBITS       000000000040a280 0000a280
     0000000000005a268 0000000000000000 A 0 0 32
  [17] .stapsdt.base    PROGBITS       00000000004e44e8 000e44e8
     0000000000000001 0000000000000000 A 0 0 1
  [18] .eh_frame_hdr    PROGBITS       00000000004e44ec 000e44ec
     0000000000003714 0000000000000000 A 0 0 4
  [19] .eh_frame        PROGBITS       00000000004e7c00 000e7c00
     00000000000012c38 0000000000000000 A 0 0 8
  [20] .gcc_except_table PROGBITS       00000000004fa838 000fa838
     00000000000000bc 0000000000000000 A 0 0 4
  [21] .tbss            NOBITS         00000000006fb5e8 000fb5e8
     0000000000000010 0000000000000000 WAT 0 0 8
  [22] .init_array       INIT_ARRAY     00000000006fb5e8 000fb5e8
     0000000000000030 0000000000000008 WA 0 0 8
  [23] .fini_array       FINI_ARRAY     00000000006fb618 000fb618

```

Figure 4.1

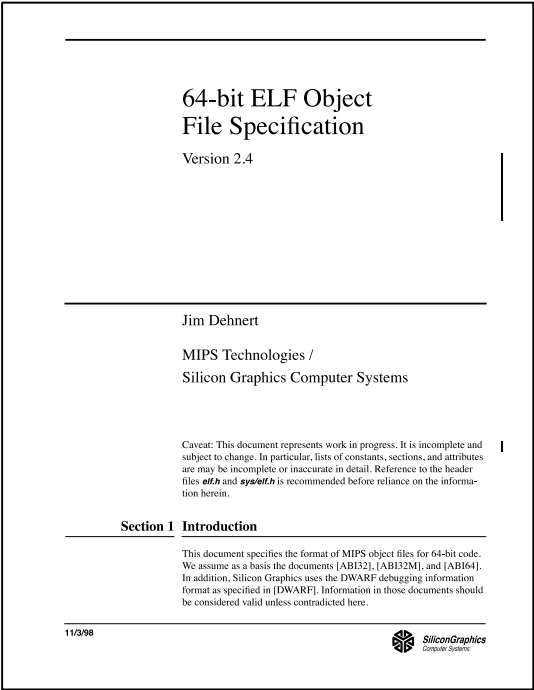


Figure 4.3

ELF-64 Data Types			
Name	Size	Alignment	Purpose
Elf64_Addr	8	8	Unsigned program address
Elf64_Half	2	2	Unsigned small integer
Elf64_Off	8	8	Unsigned file offset
Elf64_Sword	4	4	Signed medium integer
Elf64_Sxword	8	8	Signed large integer

Name	Size	Alignment	Purpose
Elf64_Word	4	4	Unsigned medium integer
Elf64_Xword	8	8	Unsigned large integer
Elf64_Byte	1	1	Unsigned tiny integer
Elf64_Section	2	2	Section index (unsigned)

Table 4.1

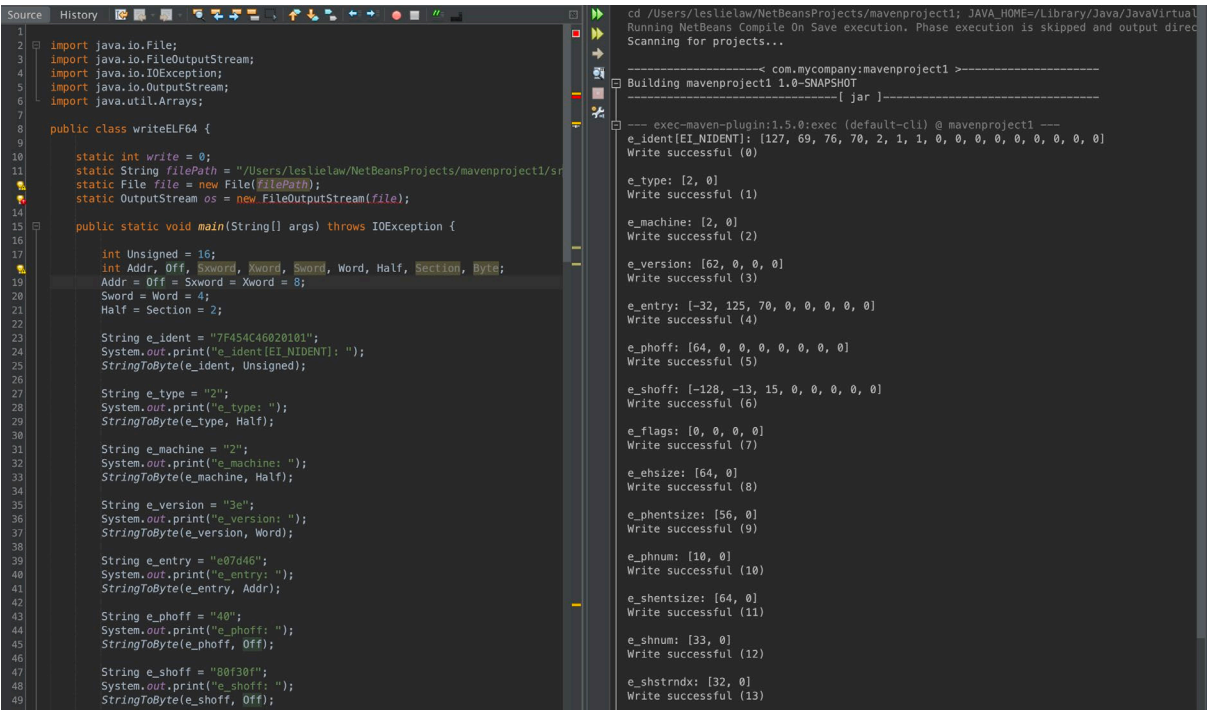


Figure 4.4

Figure 4.4 is the Java program and result of writing ELF files. It provides a way to create a customized ELF file from zero. Same as reading, the program can assign the byte into the correct position in each header which is following the specification sheet on table 4.2.

Field Name	Type	Comments
<i>e_ident</i> [<i>EL_NIDENT</i>]	unsigned char	See Table 5
<i>e_type</i>	Elf64_Half	See [ABI32]
<i>e_machine</i>	Elf64_Half	Machine (EM_MIPS = 8)
<i>e_version</i>	Elf64_Word	File format version
<i>e_entry</i>	Elf64_Addr	Process entry address
<i>e_phoff</i>	Elf64_Off	Program header table file offset
<i>e_shoff</i>	Elf64_Off	Section header table file offset

Field Name	Type	Comments
<i>e_flags</i>	Elf64_Word	Flags — see Table 6
<i>e_ehsize</i>	Elf64_Half	ELF header size (bytes)
<i>e_phentsize</i>	Elf64_Half	Program header entry size
<i>e_phnum</i>	Elf64_Half	Number of program headers
<i>e_shentsize</i>	Elf64_Half	Section header entry size
<i>e_shnum</i>	Elf64_Half	Number of section headers
<i>e_shstrndx</i>	Elf64_Half	Section name string table section header index

Table 4.2

4.3 Section Header in ELF Files

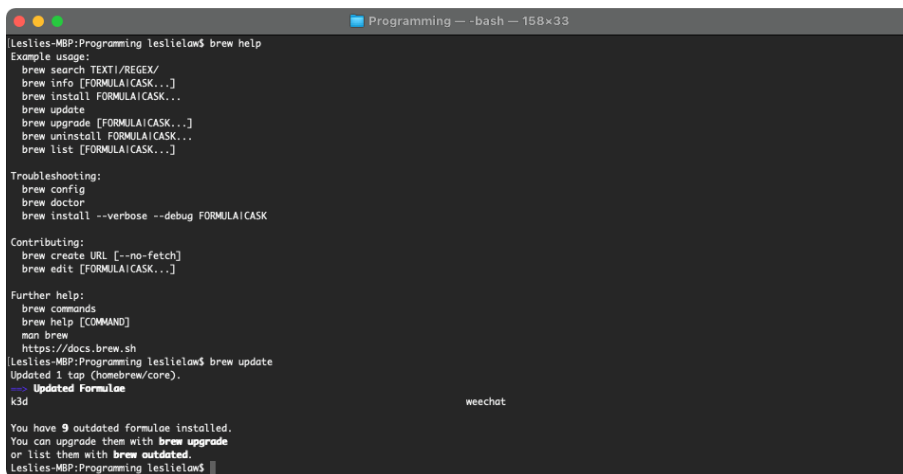
[Nr]	Name	Type	Address	Offset	
[0]	Size	EntSize	Flags	Link	Info
	0000000000000000	NULL	0000000000000000	0	0
[1]	.interp	PROGBITS	00000000400270	0000270	0
[2]	.note.ABI-tag	NOTE	0000000040028c	000028c	0
[3]	.note.gnu.bu[...]	NOTE	000000004002ac	00002ac	0
[4]	.gnu.hash	GNU_HASH	000000004002d0	00002d0	0
[5]	.dynsym	DYNYSYM	00000000400340	0000340	0

Figure 4.5

Figure 4.5 showing the first 5 fields in the section header. Each field is containing the content to be execute. Changing their order can make the data mapping in memory more efficient. If deleting the unused section, the ELF file can be more light-weighted. After analysis the section header of the GCC file, the writing ELF file program can be used to create the optimized ELF file. The new GCC file is ready for replacing the original one.

4.4 Building RISC-V Environment

Before building a RISC-V environment, Homebrew is needed which is a free and open-source software package management system that simplifies the installation of software on macOS as well as Linux. Figure 4.6 showing the help instruction and update process of Homebrew. Then, installing the RISC-V GNU Compiler Toolchain using Homebrew. Figure 4.7 showing the content of the toolchain.



```

Leslies-MBP:Programming lesliew$ brew help
Example usage:
  brew search TEXT/REGEX/
  brew info [FORMULA|CASK...]
  brew install FORMULA|CASK...
  brew update
  brew upgrade [FORMULA|CASK...]
  brew uninstall FORMULA|CASK...
  brew list [FORMULA|CASK...]

Troubleshooting:
  brew config
  brew doctor
  brew install --verbose --debug FORMULA|CASK

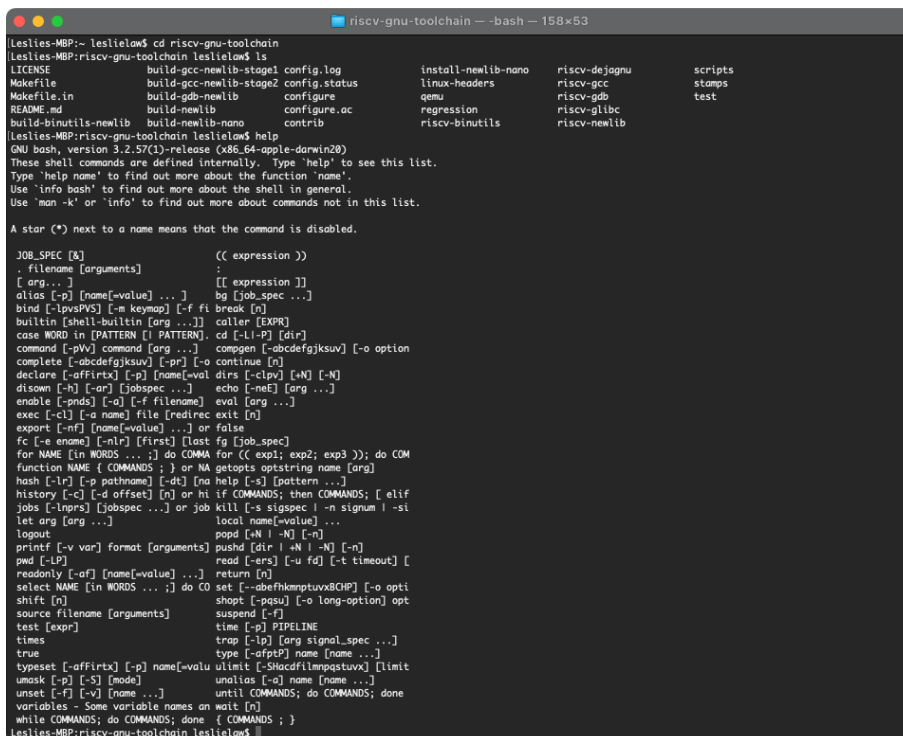
Contributing:
  brew create URL [--no-fetch]
  brew edit [FORMULA|CASK...]

Further help:
  brew commands
  brew help [COMMAND]
  man brew
  https://docs.brew.sh
(Leslies-MBP:Programming lesliew$ brew update
Updated 1 tap (homebrew/core).
Updated Formulae
k3d
wechat

You have 9 outdated formulae installed.
You can upgrade them with brew upgrade
or list them with brew outdated.
Leslies-MBP:Programming lesliew$

```

Figure 4.6



```

Leslies-MBP:~ lesliew$ cd riscv-gnu-toolchain
(Leslies-MBP:riscv-gnu-toolchain lesliew$ ls
LICENSE          build-gcc-newlib-stage1 config.log      install-newlib-nano  riscv-dejagnu      scripts
Makefile         build-gcc-newlib-stage2 config.status   linux-headers       riscv-gcc           stamps
Makefile.in      build-gdb-newlib    configure      qemu               riscv-gdb           test
README.md        build-newlib        configure.ac    regression          riscv-glibc
build-binutils-newlib build-newlib-nano  contrib         riscv-binutils     riscv-newlib

(Leslies-MBP:riscv-gnu-toolchain lesliew$ help
GNU bash, version 3.2.57(1)-release (x86_64-apple-darwin20)
These shell commands are defined internally. Type 'help' to see this list.
Type 'help name' to find out more about the function 'name'.
Use 'info bash' to find out more about the shell in general.
Use 'man -k' or 'info' to find out more about commands not in this list.

A star (*) next to a name means that the command is disabled.

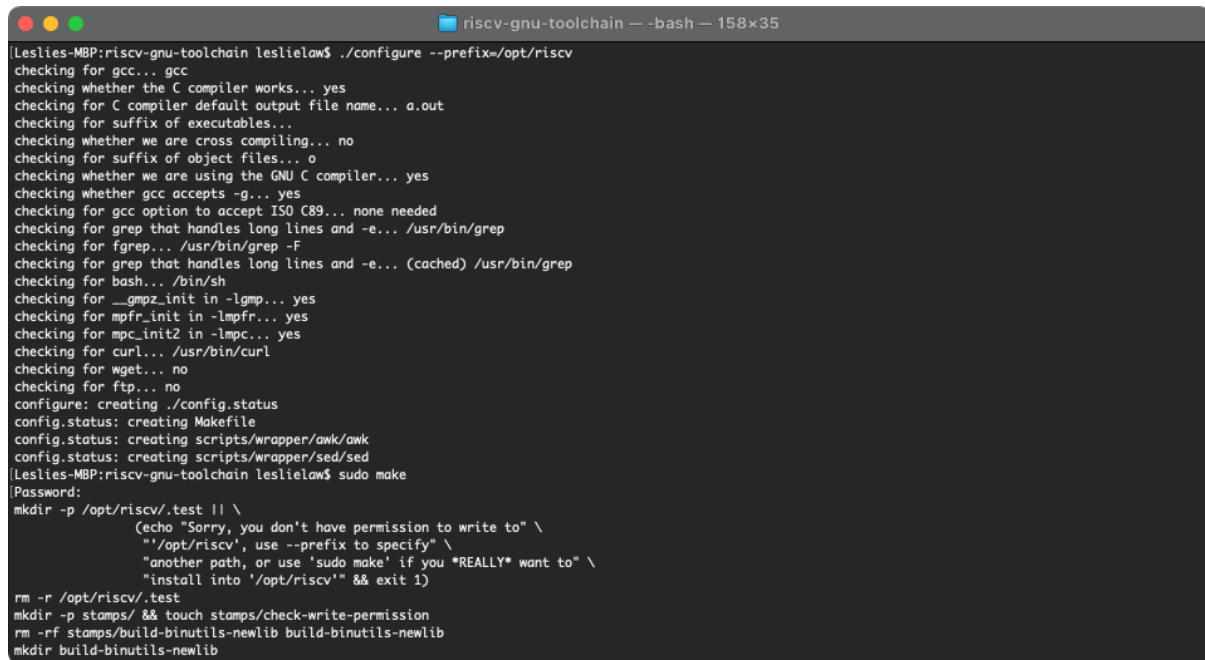
JOB_SPEC [ & ]                (( expression ))
. filename [arguments]        :
[ arg... ]                    [[ expression ]]
alias [-p] [name=value] ...   bg [job_spec ...]
bind [-lvsPSV] [= keymap]    [-f file] break [n]
builtin [shell-builtin [arg ...]] caller [EXPR]
case WORD in [PATTERN] [I PATTERN] ... cd [-L|-P] [dir]
command [-pVw] command [arg ...] compgen [-abcefgjkquv] [-o option]
complete [-abcefgjkquv] [-pr] [-o continue] [n]
declare [-affrtx] [-p] [name=value] dirs [-clpv] [+N] [-N]
dismount [-h] [-ar] [jobspec ...] echo [-neE] [arg ...]
enable [-pnps] [-a] [-f filename] eval [arg ...]
exec [-cl] [-a name] file [redirc exit [n]
export [-nf] [name=value] ... or false
fc [-e ename] [-nlr] [first] [last fg [job_spec]
for NAME [in WORDS ... ;] do COMMA for (( exp1; exp2; exp3 )); do COM
function NAME { COMMANDS ; } or MA getopts optstring name [arg]
hash [-lr] [-p pathname] [-dt] [na help [-s] [pattern ...]
history [-C] [-d offset] [n] or hi if COMMANDS; then COMMANDS; [ elif
jobs [-lnprs] [jobspec ...] or job kill [-s sigspec] -n signum l -si
let arg [arg ...]              local name[=value] ...
logout                          popd [-N] [-N] [-n]
printf [-v var] format [arguments] pushd [dir] [-N] [-N] [-n]
pwd [-LP]                      read [-ers] [-u fd] [-t timeout] [
readonly [-af] [name=value] ... return [n]
select NAME [in WORDS ... ;] do CO set [-abefhkmptuvx8CHP] [-o opti
shift [n]                      shopt [-psu] [-o long-option] opt
source filename [arguments]     suspend [-p]
test [expr]                    time [-p] PIPELINE
times                          trap [-lp] [arg signal_spec ...]
true                            type [-afptP] name [name ...]
typeset [-affrtx] [-p] name=value ulimit [-Shacdflmnpstuvx] [limit
umask [-p] [-S] [mode]         unalias [-a] name [name ...]
unset [-F] [-v] (name ...)      until COMMANDS; do COMMANDS; done
variables - Some variable names are wait [n]
while COMMANDS; do COMMANDS; done { COMMANDS ; }
Leslies-MBP:riscv-gnu-toolchain lesliew$

```

Figure 4.7

While the toolchain as known as the cross compiler is installed from Github, it is ready to build the RISC-V environment and compile the GCC. The time used to compile will be affected by the GCC file.

4.5 Compile GCC



```
Leslies-MBP:riscv-gnu-toolchain leslielaw$ ./configure --prefix=/opt/riscv
checking for gcc... gcc
checking whether the C compiler works... yes
checking for C compiler default output file name... a.out
checking for suffix of executables...
checking whether we are cross compiling... no
checking for suffix of object files... o
checking whether we are using the GNU C compiler... yes
checking whether gcc accepts -g... yes
checking for gcc option to accept ISO C89... none needed
checking for grep that handles long lines and -e... /usr/bin/grep
checking for fgrep... /usr/bin/grep -F
checking for grep that handles long lines and -e... (cached) /usr/bin/grep
checking for bash... /bin/sh
checking for __gmpz_init in -lgmp... yes
checking for mpfr_init in -lmpfr... yes
checking for mpc_init2 in -lmpc... yes
checking for curl... /usr/bin/curl
checking for wget... no
checking for ftp... no
configure: creating ./config.status
config.status: creating Makefile
config.status: creating scripts/wrapper/awk/awk
config.status: creating scripts/wrapper/sed/sed
Leslies-MBP:riscv-gnu-toolchain leslielaw$ sudo make
Password:
mkdir -p /opt/riscv/.test || \
  (echo "Sorry, you don't have permission to write to" \
    "/opt/riscv", use --prefix to specify" \
    "another path, or use 'sudo make' if you *REALLY* want to" \
    "install into '/opt/riscv'" && exit 1)
rm -r /opt/riscv/.test
mkdir -p stamps/ && touch stamps/check-write-permission
rm -rf stamps/build-binutils-newlib build-binutils-newlib
mkdir build-binutils-newlib
```

Figure 4.8

Figure 4.8 showing the compile process without editing the GCC file. Once the compiling done, the RISC-V operating environment should be ready to use. The compiling is a long process. After the first compiling done, the entire emulator file needs to be completely removed for another test.

5 Results and Discussion

5.1 GCC Compiling Result

RISC-V	32-bit	64-bit
Original GCC	32 mins 54 sec	44 mins 55 sec
Optimized GCC	30 mins 38 sec	41 mins 32 sec

Table 5.1

Table 5.1 showing the time used in compiling GCC in both 32-bit and 64-bit RISC-V setting with the original one and the optimized one. Since the compile time is very long, the time recorded is not 100% accurate, but the different is enough for comparison. For 32-bit RISC-V, the time used has decreased 6.68% which saved 2 minutes 16 second. For 64-bit RISC-V, the time used has decreased 7.57% which saved 3 minutes 23 second.

The data showed that the section header in an ELF file will affect the file execution order. The section order can be customized for different usage. The time different on a long-time consuming task will be more obvious. The lightweight GCC file make the compile time a bit shorter for building a RSIC-V environment.

6 Conclusion

The result on implementing a new optimized ELF file in RISC-V environment is as expected. The time used on compiling GCC to build RISC-V environment is decreased after using a lightweight ELF file. If doing the same thing to other ELF file for other situation in RISC-V environment, the noticeable improvement may help the future RISC-V development.

RISC-V is really a revolutionary ISA. Since it is still under development, everyone can have an opportunity to learn computer architecture from studying RISC-V. Design and make a CPU or OS is no longer exclusive for leading semiconductor and technology company.

7 References

- [1] E. Blem, J. Menon, and K. Sankaralingam, “Power struggles: Revisiting the RISC vs. CISC debate on contemporary ARM and x86 architectures,” 2013 IEEE 19th International Symposium on High Performance Computer Architecture (HPCA), 2013.
- [2] “GCC and Make,” GCC and Make - A Tutorial on how to compile, link and build C/C++ applications. [Online]. Available: https://www3.ntu.edu.sg/home/ehchua/programming/cpp/gcc_make.html. [Accessed: 13-Jun-2021].
- [3] J. Shepard, “RISC-V vs. ARM vs. x86 – What's the difference?,” Microcontroller Tips. [Online]. Available: <https://www.microcontrollertips.com/risc-v-vs-arm-vs-x86-whats-the-difference/>. [Accessed: 13-Jun-2021].
- [4] L. Lupori, V. Rosario, and E. Borin, “Towards a High-Performance RISC-V Emulator,” 2018 Symposium on High Performance Computing Systems (WSCAD), 2018.
- [5] M. Poorhosseini, W. Nebel, and K. Gruttner, “A Compiler Comparison in the RISC-V Ecosystem,” 2020 International Conference on Omni-layer Intelligent Systems (COINS), 2020.

8 Appendix

- [1] RISC-V Toolchain for macOS (Homebrew)
URL: <https://github.com/riscv/homebrew-riscv>

- [2] RISC-V GNU Compiler Toolchain
URL: <https://github.com/riscv/riscv-gnu-toolchain>

- [3] 64-bit ELF Object File Specification (Draft Version 2.5)
URL: <https://irix7.com/techpubs/007-4658-001.pdf>

- [4] Homebrew
URL: <https://brew.sh>